IN THE CLAIMS:

Please amend claims 1, 21, 25, 26, 27 and 29 as follows.

1. (Currently Amended) A nonvolatile semiconductor memory device comprising:

a memory cell array having ~~plural~~ a plurality of memory cells and arranged in an array, ~~shape by connecting these~~ the memory cells being connected to ~~plural~~ a plurality of bit lines and word lines;

~~plural~~ a plurality of address input terminals inputting a plurality of addresses thereto;

a test mode circuit for outputting a test mode signal when a signal is inputted to a predetermined terminal among ~~these~~ the address input terminals;

a row decoder connected to said test mode circuit and applying ~~a~~ an excess voltage for a test to all said word lines in response to said test mode signal;

a column decoder connected to said test mode circuit and setting all said bit lines to a non-selecting state in response to said test mode signal; and

a monitor terminal connected to said test mode circuit and outputting said test mode signal.

2. (Original) The nonvolatile semiconductor memory device according to claim 1, further comprising a select line connected to the drain of a memory cell, and a regulator connected to this select line and said test mode circuit and giving a predetermined bias electric potential to the drain of said memory cell.

3. (Original) The nonvolatile semiconductor memory device according to claim 1, further comprising a column switch connected to said column decoder and said bit line.

4. (Original) The nonvolatile semiconductor memory device according to claim 1, wherein said monitor terminal is a monitor pad.

5. (Original) The nonvolatile semiconductor memory device according to claim 1, further comprising a control signal input terminal for receiving a control signal, and a control circuit connected to this control signal input terminal.

6. (Withdrawn) A nonvolatile semiconductor memory device comprising:

a memory cell array having plural memory cells and arranged in an array shape by connecting these memory cells to plural bit lines and word lines;

plural address input terminals inputting addresses thereto;

a test mode circuit for outputting a test mode signal when a signal is inputted to a predetermined terminal among these address input terminals;

a row decoder connected to said test mode circuit and applying a voltage for a test to all said word lines in response to said test mode signal;

a column decoder connected to said test mode circuit and setting all said bit lines to a non-selecting state in response to said test mode signal; and

a monitor terminal connected to said word line and outputting the test mode signal given to said word line.

7. (Withdrawn) The nonvolatile semiconductor memory device according to claim 6, further comprising a select line connected to the drain of a memory cell, and a regulator connected to this select line and said test mode circuit and giving a predetermined bias electric potential to the drain of said memory cell.

8. (Withdrawn) The nonvolatile semiconductor memory device according to claim 6, further comprising a column switch connected to said column decoder and said bit line.

9. (Withdrawn) the nonvolatile semiconductor memory device according to claim 6, wherein said monitor terminal is a monitor pad.

10. (Withdrawn) The nonvolatile semiconductor memory device according to claim 6, further comprising a control signal input terminal for receiving a control signal, and a control circuit connected to this control signal input terminal.

11. (Withdrawn) A nonvolatile semiconductor memory device comprising:

a memory cell array having a plural memory cells and arranged in an array shape by connecting these memory cells to plural bit lines and word lines;

a test cell having plural memory cells which are connected to said word lines and are also connected to a test word line;

plural address input terminals inputting addresses thereto;

a test mode circuit for outputting a test mode signal when a signal is inputted to a predetermined terminal among these address input terminals;

a row decoder connected to said test mode circuit and applying a voltage for a test to all said word lines in response to said test mode signal;

a column decoder connected to said test mode circuit and setting all said bit lines to a non-selecting state in response to said test mode signal;

a test decoder connected to said test mode circuit and applying the voltage for a test to said test word line in response to said test mode signal; and

a monitor terminal connected to said test word line and outputting the voltage for a test applied to said test word line.

12. (Withdrawn) The nonvolatile semiconductor memory device according to claim 11, further comprising a select line connected to the drain of a memory cell, and a

regulator connected to this select line and said test mode circuit and giving a predetermined bias electric potential to the drain of said memory cell.

13. (Withdrawn) The nonvolatile semiconductor memory device according to claim 11, further comprising a column switch connected to said column decoder and said bit line.

14. (Withdrawn) The nonvolatile semiconductor memory device according to claim 11, wherein said monitor terminal is a monitor pad.

15. (Withdrawn) The nonvolatile semiconductor memory device according to claim 11, further comprising a control signal input terminal for receiving a control signal, and a control circuit connected to this control signal input terminal.

16. (Withdrawn) A nonvolatile semiconductor memory device comprising:

a memory cell array having plural memory cells and arranged in an array shape by connecting these memory cells to plural bit lines and word lines;

a test cell having plural memory cells which are connected to said word lines and are also connected to a test word line;

plural address input terminals inputting addresses thereto;

a test mode circuit for outputting a test mode signal. when a signal is inputted to a predetermined terminal among these address input terminals;

a row decoder connected to said test mode circuit and applying a voltage for a test to all said word lines in response to said test mode signal;

a column decoder connected to said test mode circuit and setting all said bit lines to a non-selecting state in response to said test mode signal;

a test decoder connected to said test mode circuit and applying the voltage for a test to said test word line in response to said test mode signal; and

a test mode detecting circuit connected to said test word line and detecting the voltage for a test applied to said test word line and outputting the detecting result.

17. (Withdrawn) The nonvolatile semiconductor memory device according to claim 16, further comprising a select line connected to the drain of a memory cell, and a regulator connected to this select line and said test mode circuit and giving a predetermined bias electric potential to the drain of said memory cell.

18. (Withdrawn) The nonvolatile semiconductor memory device according to claim 16, further comprising a column switch connected to aid column decoder and said bit line.

19. (Withdrawn) The nonvolatile semiconductor memory device according to claim 16, further comprising a control signal input terminal for receiving a control signal, and a control circuit connected to this control signal input terminal.

20. (Withdrawn) The nonvolatile semiconductor memory device according to claim 16, wherein the nonvolatile semiconductor memory device further comprises a data input -output terminal, and the detecting result of said test mode detecting circuit is outputted from said data input-output terminal.

21. (Currently Amended) A semiconductor memory device comprising:

a memory cell ~~&ray~~ array having a plurality of memory cells, a plurality of word lines and a plurality of bit lines;

a plurality of address input terminals for receiving a plurality of address signals;

a test mode circuit connected to the address input terminals, the test mode circuit providing a test mode signal in response to the address signals received thereto;

a row decoder connected to the test mode circuit and the memory cell array, the row decoder applying an excess voltage to all of the word lines in response to the test mode signal;

a column decoder connected to the test mode circuit and the memory cell array; and

a monitor terminal connected to the test mode circuit for outputting the test mode signal.

22. (Previously Presented) The semiconductor memory device according to claim 21, further comprising a regulator connected to the test mode circuit and the memory cells for providing a predetermined bias potential to the memory cells.

23. (Previously Presented) The semiconductor memory device according to claim 21 , further comprising a control circuit receiving a control signal.

24. (Previously Presented) The semiconductor memory device according to claim 21, further comprising a monitor pad connected to the monitor terminal.

25. (Currently Amended) The semiconductor memory device according to claim 21, further comprising ~~a~~ an address buffer connected to the address input terminals, the row decoder and the column decoder.

26. (Currently Amended) A semiconductor memory device comprising:

a memory cell array having a plurality of memory cells, a plurality of word lines and a plurality of bit lines;

a plurality of address Input terminals for receiving a plurality of address signals;

a test mode circuit connected to the address input terminals, the test mode circuit providing a test mode signal in response to the address signals received thereto;

a row decoder connected to the test mode circuit and the memory cell array, the row decoder ~~receiving~~ applying an excess voltage to all of the word lines in response to the test mode signal;

a column decoder connected to the test mode circuit and the memory cell, the column decoder receiving the test mode signal; and

a monitor pad connected to the test mode circuit for outputting the test mode signal.

27. (Currently Amended) The semiconductor memory device according to claim ~~28~~ 26, further comprising a regulator connected to the test mode circuit and the memory cell array for providing a predetermined bias potential to the memory cells.

28. (Previously Presented) The semiconductor memory device according to claim 26, further comprising a control circuit receiving a control signal.

29. (Currently Amended) The semiconductor memory device according to claim 26, further comprising ~~a~~ an address buffer connected to the address input terminals, the row decoder and the column decoder.